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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,106	02/19/2002	Kerry D. Tedrow	42390P9670D	4543
8791	7590	12/16/2003		
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025				
EXAMINER				
NGUYEN, VAN THU T				
ART UNIT		PAPER NUMBER		
2824				

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/078,106	Applicant(s) TEDROW ET AL.	
	Examiner VanThu Nguyen	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Response to Election 9/19/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 25-39 and 48-51 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 25-39 and 48-51 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 18 July 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>08212003</u> . | 6) <input checked="" type="checkbox"/> Other: <u>Search Report</u> . |

DETAILED ACTION

1. Claims 25-39 and 48-51 are present for examination.
2. Claims 40-47 are cancelled.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 48-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Amanai (U.S. Patent No. 5,787,037).

Regarding claim 48, Amanai discloses an apparatus comprising:

a negative charge pump (57, see FIG. 2);

a block controller (comprising 52, 55, 56) coupled to the negative charge pump comprising:

a negative level shifter (55, see FIG. 2, and detail circuitry in FIG. 4) to switch an output between a read-mode voltage and an erase-mode voltage dependent upon a selection signal input (Con2, see FIG. 2) (see column 8, line 56 to column 9 line 2); and

a positive voltage switch (56, see FIG. 2) coupled to the negative level shifter.

Regarding claim 49, Amanai further discloses, in FIG. 4, the negative level shifter comprises an output stage circuit (comprising Tp8, Tn8, Tp9, Tn9) to couple to said negative charge pump (via Vin) to output the erase-mode voltage (V_{ss}/V_{cc}).

Regarding claim 50, Amanai also discloses, in FIG. 5, the negative level shifter comprises a first circuit (comprising Tp8, Tn8, Tp9, Tn9) to pull up an output of said negative charge pump to output a read-mode voltage (V_{cc}/V_{ss}).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 25-31, 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amanai in view of Sawada et al. (U.S. Patent No. 5,557,572)

Regarding claim 25, Amanai disclose a system comprising:

a memory array (51, see FIG. 2);

a negative charge pump (57, see FIG. 2);

a block controller (comprising 52, 55, 56) coupled to the negative charge pump

comprising:

a negative level shifter (55, see FIG. 2, and detail circuitry in FIG. 4) to

switch an output between a read-mode voltage and an erase-mode voltage

dependent upon a selection signal input (Con2, see FIG. 2) (see column 8, line 56

to column 9 line 2);

a positive voltage switch (56, see FIG. 2) coupled to the negative level shifter;

a word line driver (522, see FIG. 2) coupled to said positive voltage switch (via 521), coupled to the negative level shifter (via 521), and coupled to said memory array.

However, Amanai does not disclose a bit line driver coupled to the positive voltage switch and coupled to said memory array.

Sawada et al. disclose, in FIG. 4, bit line drivers (M5-M8) coupled to a positive voltage switch (HVSW3) and coupled to a memory array (MBLK).

Since Amanai and Sawada et al. are both from the same field of semiconductor, the purpose disclosed by Sawada would have been recognized in the pertinent art of Amanai.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to supply bit line drivers of a memory array with positive voltage for the purpose of perform operations on the memory array such as read/write/erase.

Regarding claims 26-31, 33-36, all the other limitations listed are well known. It would have been obvious to add known elements in order to add known functions.

7. Claims 32, 37-39, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amanai in view of Sawada et al. further in view of Thummalapally et al. (U.S. Patent No. 6,016,270).

Regarding claim 32, Amanai in view of Sawada et al. disclose, as applied in prior rejection of claim 25, all claimed subject matter except further limitation in claim 32.

Thummalapally et al. disclose, in FIG. 1, a memory device comprises a plurality of blocks (14), and each block comprises a block controller, to apply a signal to second block within said memory array to read a memory cell of the second block substantially simultaneously with erasure of a first block within said memory array (see column 4, lines 9-33).

Since Amanai, Sawada et al., and Thummalapally et al. are all from the same field of semiconductor, the purpose disclosed by Thummalapally et al. would have been recognized in the pertinent art of Amanai and Sawada et al.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to perform erase and read operations simultaneously on different blocks in a memory array in order to improve performance of the memory device.

Regarding claims 37 and 51, it would have been obvious for Thummalapally et al. to design a block controller having elements as disclosed in Amanai for the for purpose of controlling performance of read/write/erase in each block separately.

Regarding claims 38-39, all the other limitations listed are well known. It would have been obvious to add known elements in order to add known functions.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (703) 306-9121. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Art Unit: 2824

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VTN
December 11, 2003



VanThu Nguyen
Primary Examiner
Art Unit 2824